Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

What is claimed is:

1. – 12. (Canceled)

13. (Currently Amended) The device according to, claim [[1]] 16, wherein the load further comprising cascoded transistors comprise NMOS transistors, and the amplifying means and the tail-current source comprises PMOS transistors.

14. (Previously Presented) The device according to claim 13, wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source, and the width-over-length ratio of the second transistor pair of the load is at least 3 times the size of the width-over-length ratio of the first transistor pair of the load.

15. (Previously Presented) The device according to claim 13, wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair of the load is in the range of 2.5-125 μm, and the length of the transistors is in the range of 0.25-12.5 μm; the width and the length of the transistors of the tail-current source and the transistors of the first transistor pair of the load are in the range of 0.25-12.5 μm.

16. (Currently Amended) ~~The device according to claim 1~~ A device for generating a noise signal, comprising:

a noise source for generating intrinsic noise, the noise source further comprising:

a noisy amplifier cell having amplifying means, wherein input terminals of the amplifying means of the noisy amplifier cell are short-circuited AC-wise to a grounding means;

a load further comprising cascoded transistors coupled to the amplifying means and a power supply; and

a tail-current source coupled to the grounding means and to the amplifying means.

17. (Canceled)

18. (Currently Amended) ~~The device according to claim 7, further comprising: the,~~ A device for generating a noise signal, comprising:

a noise source for generating intrinsic noise, the noise source further comprising: a noisy amplifier cell having amplifying means;

a first amplifier cell being DC coupled to the noisy amplifier cell;

the output terminals of the noisy amplifier cell coupled to respective input terminals of the first amplifier;

a DC compensation loop having a feedback filter coupled to the output terminals of the first amplifier and to the input terminals of the noisy amplifier, respectively;

a load further comprising cascoded transistors coupled to the amplifying means and a power supply; and

a tail-current source coupled to grounding means and to the amplifying means.

19. (Previously Presented) The device according to claim 18, wherein the feedback filter comprises first and second filters each comprising a high-frequency phantom zero capacitor providing phase compensation.

20. (Previously Presented) The device according to claim 18, wherein the feedback filter comprises two filters each comprising a first capacitor coupled to grounding means and a first resistor coupled to the output terminal of the filter, a second

resistor in parallel to the high-frequency phantom zero capacitor coupled to the output terminal of the filter and to a third resistor being coupled to the input terminal of the filter.

21. (Previously Presented) The device according to claim 20, wherein the first capacitor, the first resistor, the second resistor, the high-frequency phantom zero capacitor, and the third resistor comprises MOS transistors.

22. (Previously Presented) The device according to claim 20, wherein the first capacitor comprises NMOS transistors, and the first resistor, the second resistor, and the third resistor comprises PMOS transistors.

23. (Previously Presented) The device according to claim 20, wherein the first capacitor comprises PMOS transistors, and the first resistor, the second resistor, and the third resistor comprises NMOS transistors.

24. (Currently Amended) The device according to claim [[1]] 18, further comprising:

a noise source output terminal;

a random generating sequence device for generating a random sequence of bits coupled to the noise source output terminal;

the random generating sequence device further comprising:

oscillating means having an input terminal for receiving a bias as input, the oscillating means coupled to the noise source output terminal, the oscillating means further comprising at least one oscillator amplifier; amplifying means comprising at least one a differential amplifier coupled to a corresponding the at least one oscillator amplifier;

a load coupled to the amplifying means and to a power supply, the load being adapted to protect the amplifying means from interfering signals; and

a tail current source coupled to the amplifying means and grounding means.

25. (Currently Amended) The device of claim [[1]] 18, further comprising an electronic apparatus for generating a noise signal.

26. (Previously Presented) The device according to claim 25, wherein the electronic apparatus is one from the group consisting of a mobile radio terminal, a pager, a communicator, an electronic organizer and a smartphone.

27. (Previously Presented) The electronic apparatus according to claim 25, wherein the apparatus is a mobile telephone.

28. (Currently Amended) The device according to claim [[1]] 18, the device being fabricated on an integrated circuit.

29. (Currently Amended) The device according to claim [[12]] 18, wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source, and the width-over-length ratio of the second transistor pair of the load is at least 3 times the size of the width-over-length ratio of the first transistor pair of the load.

30. (Currently Amended) The device according to claim [[12]] 18 wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair of the load is in the range of 2.5-125 μm, and the length of the transistors is in the range of 0.25-12.5 μm; the width and the length of the transistors of the tail-current source and the transistors of the first transistor pair of the load are in the range of 0.25-12.5 μm.

31. (New) The device according to claim 16, wherein the gate-over-drive voltage of the amplifier means is approximately 100mV.

32. (New) The device according to claim 18, wherein the gate-over-drive voltage of the amplifier cell is approximately 100mV.